

YO998-426DIV

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re divisional patent application of

Chan et al.

Serial No.: Not yet assigned

Group Art Unit: Unknown

Filed: Concurrently herewith

Examiner: Unknown

For: SELF-ALIGNED DOUBLE-GATE MOSFET BY SELECTIVE EPITAXY
AND SILICON WAFER BONDING TECHNIQUES

Assistant Commissioner of Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to examination on the merits and calculation of the filing fee, please amend the
above-identified application as follows:

IN THE SPECIFICATION:

Page 1, after line 3, insert the following:

-- Cross-Reference To Related Applications

This application is a division of U.S. Application Serial Number 09/272,297 filed
March 19, 1999. --

Please replace the paragraph appearing on page 4, lines 11-16 of the application with
the following paragraph.

There are two different issues important to this aspect of the invention. First the
introduction of impurities is for the purpose of limiting the diffusion. For example,
introduction of carbon reduces boron diffusion. Secondary, forming an alloy such as $\text{Si}_x\text{Ge}_{1-x}$

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in the drain and source regions, is a band-gap engineering technique. For example, a $\text{Si}_x\text{Ge}_{1-x}$ source will allow a more efficient sinking of "holes" generated in the channel, thus reducing the "kink effect".

Please replace the paragraph appearing on page 7, lines 13 - 14, of the application with the following paragraph:

Figures 3A-3D are schematic diagrams that illustrate another embodiment of the invention;

Please replace the paragraph appearing on page 7, lines 19 - 20, of the application with the following paragraph:

Figures 6A-6E are schematic diagrams that illustrate another embodiment of the invention that forms a sidewall spacer;

Please replace the paragraph appearing on page 18, lines 9 - 17, of the application with the following paragraph:

A reactive ion etch is employed, as discussed above, to form a spacer 21, as shown in Figure 6B. Figures 6C and 6D illustrate the result of an isotropic etching process (e.g., reactive ion etching or wet chemical etching) performed to remove residues 22 of the spacer dielectric 21 from the exposed silicon sidewall of the SOI channel 5. Then, as shown in Figure 6E, amorphous silicon 31 is deposited to form the source/drain regions. Alternatively, epi silicon may be re-grown from the exposed SOI channel extension 16 to fill up the drain and source regions. The remainder of the fabrication process is similar to the process discussed above with respect to Figures 2A-2BB.

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IN THE CLAIMS:

Please cancel claims 1-17 without prejudice or disclaimer.

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REMARKS

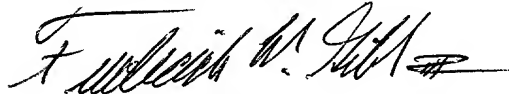
The above changes to the claims have been made to cancel claims being prosecuted in a separate application. This Preliminary Amendment leaves claims 18-24 pending in the present application.

The prior application is assigned of record to International Business Machines Corp., Armonk, New York, at Reel 009843, Frame 0970.

Early and favorable prosecution on the merits is respectfully requested.

Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-0510.

Respectfully submitted,



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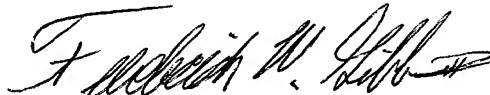
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SUBMISSION OF FORMAL DRAWINGS

Sir:

Submitted herewith are twenty-five (25) sheets of formal drawings comprising Figs. 1A-8
for the above-referenced patent application. Acknowledgment of receipt is respectfully requested.
Please substitute these formal drawings for the drawings which were filed with the application.

Respectfully Submitted,



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